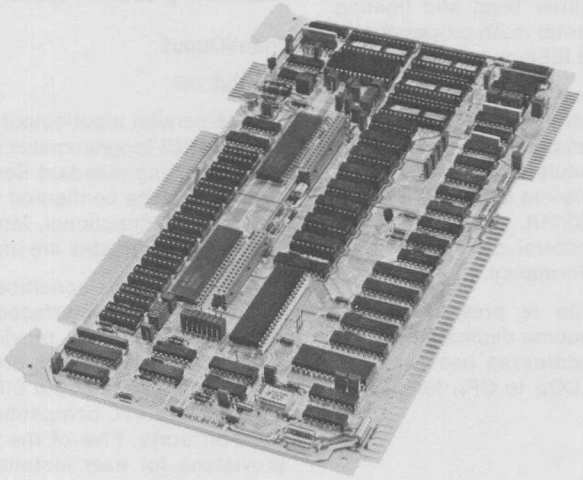
National Semiconductor

BLC-80/11A, BLC-80/14A Series/80 Board Level Computers



- **Upward compatible with BLC-80/11 board level computer**
- **Two BLX bus connectors for on-board expansion with BLX series modules**
- **1 K and 4 K bytes of RAM**
- **Sockets for up to 32 K bytes of PROM**
- **48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators**
- **Programmable synchronous/ asynchronous communications port with selectable RS-232C or 20 mA current loop interface**
- **Single level interrupt with 16 interrupt sources**
- **Auxiliary power bus and power-fail interrupt control logic for RAM battery backup**
- **Limited master Multibus™ interface**
- **Compatible with industry standard BLC/SBC Series/80 hardware and software**
- **Plug replacement for SBC-80/10B**

Product Overview

The BLC-80/11A Family of Board Level Computers (BLC-80/11A, BLC-80/14A) are members of a family of Series/80 products with the BLX interface. This interface (identical to the SBX standard) provides the means for economical expansion of on-board resources. The OEM can combine the BLC-80/11A with any of the BLX series of expansion modules and customize his application with off-the-shelf products from National Semiconductor Corporation.

The BLC-80/11A Family is essentially the BLC-80/11 Family (BLC-80/11, BLC-80/14) with several enhancements. These, in general, include two BLX connectors, support for 2764 PROMs, and battery backup logic.

Multibus is a trademark of Intel Corp.

Functional Description

BLX Module Expansion Bus

The new BLX bus interface brings an entirely new dimension to system design, offering incremental, on-board expansion with small BLX modules. Two BLX bus connectors are provided to allow plug-in expansion with any BLX module. One may use these to expand existing on-board resources, or configure entirely new functions.

Examples of expanding existing BLC-80/11A resources would be adding the BLX-350 Parallel I/O Module, or the BLX-351 Serial I/O Module. These provide respectively 24 additional programmable parallel I/O lines, with sockets for user customization of

the interface, and an additional synchronous/asynchronous serial port, either RS-232C or RS-449/442.

A means of adding new functionality would be to install the BLX-331 or BLX-332 Math Processor Modules. These provide either fixed and floating point math with transcendental math processing or floating point math with the IEEE-suggested format.

The BLX module is a logical extension of the on-board programmable I/O, and is accessed by the BLC-80/11A Board Level Computer as a common I/O port location. The BLX module is coupled directly to the 8080A CPU, and therefore becomes an integral element of the BLC-80/11A. This negates the need for contending for control of the Multibus, providing for optimum performance.

Only when a BLX module is present do the assigned I/O addresses become dedicated to that BLX connector. The I/O addresses used when a module(s) is installed are CO_H to CF_H for J4 and FO_H to FF_H for J5.

Central Processor

The INS8080A N-channel LSI microprocessor is the central processor for the BLC-80/11A. The INS8080A contains six general purpose 8-bit registers, an 8-bit accumulator, a 16-bit stack pointer register, and a 16-bit program counter.

The six general purpose registers can be utilized singly or in pairs when double precision operations are required.

The 16-bit program counter allows direct addressing of a full 64 K-bytes of memory. The 16-bit stack pointer allows the user's stack to be located anywhere within the 64 K memory space. This concept of locating a user's stack in system memory allows unlimited subroutine nesting levels and the flexibility of maintaining multiple stack areas.

Memory

The BLC-80/11A, and BLC-80/14A are shipped with 1 K-byte and 4 K-bytes, respectively, of static RAM. RAM starting address is jumper-selectable to begin immediately after PROM, regardless of the amount of PROM installed, or on any boundary defined by the amount of RAM installed. All on-board RAM read and write operations are performed at maximum processor speed.

Four 28-pin sockets are provided to allow user installation of read only memory for specific applications. Allowable device types are 1 K × 8 (2708, 2758), 2 K × 8 (2716), 4 K × 8 (2732), and 8 K × 8 (2764), or pin compatible ROMs. This provides on-board installation of as much as 32 K-bytes of permanent storage. If less than four devices are present, jumpers allow dedication of the unused space to other resources. All on-board ROM, or EPROM, read operations are performed at maximum processor speed.

Input/Ouput

Parallel I/O

The 48 parallel input/output lines are controlled by two INS8255 Programmable Peripheral Interface (PP) devices. Using standard Series/80 instructions, the 48 lines may be configured to a wide variety of unidirectional/bidirectional, latched/unlatched modes. The operating modes are defined in Appendix B.

The I/O section is specifically designed to permit the lines to be interfaced to a wide range of devices. Sockets are provided to allow matching line characteristics with driver and terminator circuits contained in 14-pin DIP packages. All parallel I/O lines are TTL compatible and are divided into six 8-bit ports. Five of the six parallel ports have provisions for user installed driver or terminator modules. Port 1 has a permanently installed 8303 type driver. Figure 1 illustrates the I/O address assigned to the 8255 PPI's.

Figure 1. I/O Addresses

	8255 No. 1				8255 No. 2			
Port	**1**	**2**	**3**	**Control**	**4**	**5**	**6**	**Control**
Address*	E4	E5	E6	E7	E8	E9	EA	EB

*Hexadecimal notation

National's BLC-901 and BLC-902 terminator modules, as well as a number of TTL devices, are available to satisfy a variety of requirements. The BLC-901 contains 220/330 ohm divider type terminator circuits for four lines, while the BLC-902 contains 1 K ohm pull-ups for four lines. Figure 2 illustrates the terminator circuit configuration and Table I lists the compatible driver modules.

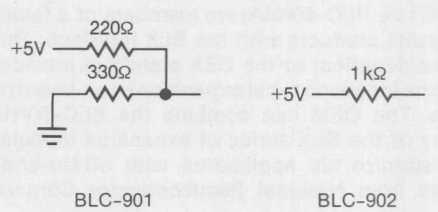


Figure 2. BLC-901 and BLC-902 Terminators

Table I. Compatible I/O Driver Modules

Type	Output	Current (mA)
7400	I	16
7403	I, OC	16
7408	NI	16
7409	NI, OC	16
7426	I, OC, HV	16
7432	NI	16
7437	I	48
7438	I, OC, HV	48

(I = inverting; NI = non-inverting; OC = open collector; HV = high voltage)

Serial I/O

One INS8251 Universal Synchronous/ Asynchronous Receiver Transmitter (USART) provides the serial I/O port with programmable communications rates, data formats, control characters, and parity. Logic is provided for detection of framing, overrun, and parity errors as well as double buffering. The serial I/O port can be jumper selected to RS-232C standards or 20 mA current loop, and interfaces via a 26-contact edge connector. The data interface is located at I/O address EC_H, control at ED_H. Table II lists the serial baud rates available.

Table II. Serial Baud Rates

Baud Rate Clock (user selectable) (KHz)	Baud Rate (Hz)		
	Synchronous	Asynchronous (program selectable)	
		÷16	÷64
307.2	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
3.49	3490	—	110

Interrupt System

Interrupt requests may originate from 16 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Three jumper selectable interrupt requests can automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), a character is ready to be transmitted (i.e. the USART is ready to accept a character from the CPU), or when the transmitter is empty (i.e., the USART has no character to transmit). These five interrupt request lines are all maskable under program control. Two interrupt request lines may be interfaced directly to user designated peripheral devices; one via the Multibus system bus and the other via the I/O edge connector. One jumper selectable interrupt request may be interfaced to the power-fail interrupt control logic. Two general purpose and two optional interrupt requests are jumper selectable from each of the BLX interfaces. These eight signals permit user installed expansion modules to interrupt the 8080A CPU. The sixteen interrupt request lines share a single CPU interrupt level. When an interrupt request is recognized, a restart instruction (RESTART 7) is generated. The processor responds by suspending program execution and executing user defined interrupt service routine originating at location 38_H.

Power-Fail Circuitry

A power-fail interrupt may be detected through the AC-low signal generated by the power supply. This signal may be configured to interrupt the 8080A CPU to initiate an orderly power down instruction sequence. Additionally, if battery backup power is being supplied through the auxiliary connector (P2), read and write operations to RAM are disabled, and RAM contents are maintained.

Specifications

Microprocessor

CPU — INS8080A

Data Word — 8 bits

Instruction Word — 8, 16, 24 bits

Cycle Time — 1.95 microseconds (minimum instruction time)

System Clock — 2.048 MHz ± 0.1%

Registers — 6 General Purpose, 8-bit Accumulator, 8-bit Program Counter, 16-bit Stack Pointer, 16-bit

Number of Instructions — 111

Address Capacity — 64 K bytes

Memory

RAM — BLC-80/11A — 1 K bytes
BLC-80/14A — 4 K bytes

ROM/PROM — Sockets for up to 32 K bytes

RAM Memory Addressing — Any boundary within $FFFF_H$ where boundary defined by amount of RAM installed (i.e. if 2 K bytes installed, locate on any 2 K byte boundary)

ROM Memory Addressing — 0_H-$0FFF_H$ using 2708, 2758
0_H-$1FFF_H$ using 2716
0_H-$3FFF_H$ using 2732
0_H-$7FFF_H$ using 2764
(Assuming all sockets used)

Off-Board Expansion — Memory boards in any mix of RAM and ROM/PROM up to a system total of 64 K bytes

Input/Output

Interrupts — Single level, 16 sources
- 2 — User specified I/O
- 2 — Parallel I/O
- 3 — Serial I/O
- 1 — Power-fail interrupt
- 8 — BLX connectors (2)

Parallel — 48 lines
Latched, unlatched, strobed modes
4- and 8-bit parallel configuration
Optional line drivers and terminators
TTL compatible

Serial — 20 mA current loop or RS-232C

Synchronous Mode — 5-8-bit character
Internal/external synchronization
Automatic SYNC insertion
SYNC search

Asynchronous Mode — 5-8-bit character
1, 1½, or 2 stop bits
False start bit detect
Break character generation

BLX Expansion — 2 BLX expansion connectors. Accepts 2 single-size or 1 double size BLX module.

I/O Addressing — (On-board programmable I/O)

Device	I/O Address
8255 No. 1	
Port A	E4
Port B	E5
Port C	E6
Control	E7
8255 No. 2	
Port A	E8
Port B	E9
Port C	EA
Control	EB
8251	
Data	EC
Control	ED
BLX Connector J4	
MCS0	C0-C7
MCS1	C8-CF
BLX Connector J5	
MCS0	F0-F7
MCS1	F8-FF

Connectors

System Bus — 86-contact double-sided card cage edge connector on 0.156-inch centers

Auxiliary — 60-contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
CDC VPB01B30A00A2
AMP PES-14559

Parallel I/O — 50-contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M 3415-0001
AMP 2-86792-3

Serial I/O — 26-contact double-sided edge connector on 0.1-inch centers
Recommended mating connector:
3M 3462-001 flat
AMP 2-86792-3 round

Power —

VDC	Normal	Battery
+5 V ± 5%	3.46 A	25 mA + 140 mA/ KB RAM
−5 V ± 5%	2 mA	—
+12 V ± 5%	150 mA	—
−12 V ± 5%	175 mA	—

Note 1: Based on the following installed: four 2758, 2716, or 2732 EPROMs, 1 KB of RAM, BLC-901 on 48 input lines (inputs low)

Environmental Temperature — 0° to 55°C
Humidity — 0% to 90%, non-condensing

Physical Height: 6.75 in. (17.15 cm)
Width: 12.00 in. (30.48 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 14 oz. (396.9 g)

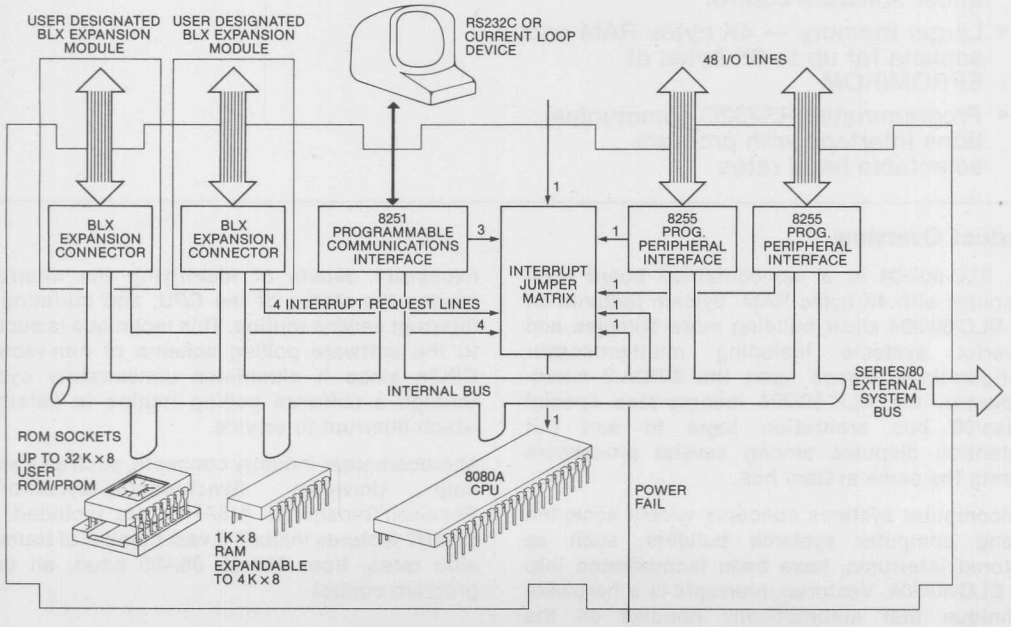
Order Information

BLC-80/11A — Series/80 Board Level Computer Includes CPU, 1 K bytes of static RAM, sockets for up to 32 K bytes of ROM, 48 parallel I/O lines, one serial port and 2 BLX expansion connectors.

BLC-80/14A — Series/80 Board Level Computer Includes CPU, 4 K bytes of static RAM, sockets for up to 32 K bytes of ROM, 48 parallel I/O lines, one serial port, and 2 BLX expansion connectors.

Documentation

420306321-001 — BLC-80/11A, BLC-80/14A Board Level Computer Hardware Reference Manual



BLC-80/11A Block Diagram